VASAVI COLLEGE OF ENGINEERING (*Autonomous*), HYDERABAD
B.E. (CSE) II Year I-Semester Backlog Examinations, December-2017
Logic & Switching Theory

Time: 3 hours

Max. Marks: **70**

*Note: Answer ALL questions in **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

1. Convert the Decimal number 53.125 to Binary and Hexa decimal number systems.
2. Find the compliment of the following expression (x'+y+z')(x+y')(x+z).
3. Why are NAND and NOR gates called "Universal gates"?
4. What are the advantages of tabulation method over Karnaugh map method of simplifying logic functions?
5. Draw the truth table for a Priority Encoder.
6. Implement a half adder circuit using minimum number of NAND gates.
7. Differentiate a Moore model from a Mealy model?
8. Write the Characteristic tables of JK & T Flip flops.
9. Differentiate between different types of counters.
10. Draw the circuit diagram of a 4 bit serial shift register.

Part-B (5 × 10 = 50 Marks)

11. a) List down any six theorems or postulates of Boolean Algebra. Prove Demorgan's theorem using truth table. [6]

    b) Express the following function as a sum of minterms and as a product of maxterms: [4]
    F(A,B,C,D)=B'D+A'D+BD

12. a) Explain the steps of converting two level and multilevel circuit diagrams consisting of any logic gates to circuits consisting of only NAND gates. [4]

    b) Simplify the following function using Tabular method and draw the logic circuit diagram with NAND gates. [6]
    F(A, B, C, D) = Σ(1, 2, 3, 5, 7, 9, 10, 11, 13, 15)

13. a) Design a 4-input priority Encoder with a minimum number of gates. [5]

    b) Implement the Boolean function F(A,B,C,D) = Σ(1,3,4,11,12,13,14,15) with a 8 to 1 Line multiplexer and external gates. [5]

14. a) Explain the behaviour of an SR latch using circuit diagram and truth table. How can a SR master slave flip flop be designed from SR latches? [6]

    b) A sequential circuit has two JK flipflops A and B, two inputs x and y and output z. The flip flop input equations and circuit output equations are given as follows: [4]
    $J_A = Bx+B'y'$ $K_A = B'xy'$
    $J_B = A'x$ $K_B = A+xy'$
    $Z = Ax'y'+Bx'y'$
    Draw the logic circuit diagram of the circuit

15. a) Explain the working of a 4 bit register having parallel load capability with the help of a circuit diagram. [6]

   b) Design a Synchronous sequential counter that follows the state sequence. 0, 1, 3, 6, 7, 5, 4, 2 using JK Flip flops. [4]

16. a) What is the underlying principle of minimization of Boolean functions using a Karnaugh Map? Explain the method of using Karnaugh maps to minimize Boolean functions. [5]

   b) Simplify the following function using k-map method and draw the circuit diagram.
   $F(a.b,c,d) = \sum m(0,1,2,4,5,8,10,11,14)$ [5]

17. Answer any *two* of the following:

   a) Design a full adder using a decoder. [5]

   b) Explain the design procedure of sequential circuits. [5]

   c) Design a BCD counter. [5]

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